UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,564	07/10/2003	Luigi Di Gregorio	021111-000800US	3753

20350 7590 11/20/2006

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,564	DI GREGORIO, LUIGI	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10,12,14-19 and 22* is/are rejected.

7)☐ Claim(s) *6-8,11,13,20,21 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/05, 4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 9/22/05 was considered.

2. Claims 1-23 are presented for examination.

Claim Objections

3. Claim 3 is objected to because a limitation of "a second pull up transistor" is claimed without first claiming a first pull up transistor. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper form.

Claim Rejections - 35 USC ∋ 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9-10, 12, 14-19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al, Pat. No. 6292401.

With regard to claim 1, Zhang discloses a memory array circuit comprising: memory cells (fig. 4, memory in column 401 and 402) first read bit lines (fig. 4, 416, 418) coupled to a first subset of the memory cells (fig. 4, memory in column 401); and first NAND gates (fig. 4, NAND gate locate between bit line 416 and 418) coupled to the first

read bit lines (fig. 4, 416 and 418), wherein each of the first NAND gates has two inputs that are coupled to two of the first read bit lines (fig. 4, the NAND gate that receives bit line 416 and bit line 418 as their two inputs).

With regard to claim 2, Zhang discloses first transistors, each having an input coupled to an output of one of the first NAND gates (fig. 4, the transistor having it's gate coupled to the output of the NAND gate that couple to the bitline 416 and 418); and a first global bit line couple to each of the first transistor (fig. 4, 405).

With regard to claim 3, Zhang discloses a second pull up transistor coupled to the first global bit lines (fig. 4, the transistor whose gate received a CK clock signal) (col. 3, line 23-30); and third pull up transistor, each are coupled to one of the first read bit lines (fig. 4, the transistor that connected to the top of the bit line 416 in column 401), and the first transistor are pull down transistors (col. 4, line 1-8).

With regard to claim 4, Zhang discloses second read bit lines (fig. 4, 422 and 424) coupled to a second subset of the memory cells (fig. 4, memory cells in column 402); and second NAND gates coupled to the second read bit line (fig. 4, NAND gate coupled to bit line 422 and 424), wherein each of the second NAND gates has two inputs that are coupled to two of the second read bit lines (fig. 4, read bit line 422 and read bit line 424 are the two bit lines coupled to the two inputs of the NAND gate).

With regard to claim 5, Zhang discloses second transistors, each of the second transistor having an input coupled to an output of one of the second NAND gates (fig. 4, the transistor receiving output of the NAND gates that receives bit line 422 and 424); and a second global bit line (fig. 4, 410) coupled to each of the second transistors.

With regard to claim 9, Zhang discloses a memory array circuit comprising: memory cells (fig. 4, memory in column 401 and 402) first read bit lines (fig. 4, 416, 418) coupled to a first subset of the memory cells (fig. 4, memory in column 401); and first logic gates (fig. 4, NAND gate locate between bit line 416 and 418), each coupled to receive signals on two of the first local read bit lines (fig. 4, the NAND gate that receives read bit line 416 and read bit line 418 are their two inputs); a first global bit line (fig. 4, 405); and first transistors (fig. 4, the transistor that received the output signal of the NAND gate that is coupled to the bit line 416 and 418) coupled between the first global bit line (fig. 4, 405) and the first logic gates (fig. 4, the NAND gate that received bit line 416 and 418).

With regard to claim 10, Zhang discloses second read bit lines (fig. 4, 422 and 424) coupled to a second subset of the memory cells (fig. 4, memory cells in column 402); and second logic gates (fig. 4, NAND gate that coupled to the bit line 422 and 424), each coupled to received signals on two of the second local bit lines (fig. 4, read bit line 422 and read bit line 424); a second global bit line (fig. 4, 410); and second transistors (fig. 4, the transistor that receives the output of the NAND gates that couple to the bitlines 422 and 424) coupled between the second global bit lines (fig. 4, 410) and the second logic gates (fig. 4, the NAND gate that coupled to the bitline 422 and 424).

With regard to claim 12, Zhang discloses wherein the first logic gates and the second logic gates are NAND gates (fig. 4, NAND gates that receives bit line 416 and 418 and NAND gates that receives bit line 422 and 424)

With regard to claim 14, Zhang discloses a first pre-charge transistor (fig. 4, transistor connected to global bit line 405 that receives clock signal CK); and a plurality of second pre-charge transistors that are each coupled to one of the first local read bit lines (fig. 4, transistor connected to bit line 416 and transistors connected to bit line 417) (col. 3, line 22-29).

Drafted as Method claim

5. As per claim 15-19 and 22 encompass the same scope of invention as to that of claim 1-5, 9-10, 12 and 14 except they are draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Allowable Subject Matter

6. Claim 6- 8, 11, 13, 20-21 and 23 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of a third NAND gate having a first input coupled to the first global bit lines and a second input coupled to the second global bit line or that a repeater circuit coupled between the first global bit line and the second global bit line.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Khellah et al (US 2004/0139271 A1), Chehrazi et al (6654301), Song et al (6614710) and Desai et al (6597611) disclose a memory device having Nand gates receiving two local bitlines similar to the instant invention.

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

November 2006

Connie C. Yoha

Art Unit 2827

CONNIE C. YOHA
PRIMARY EXAMINER